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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,841	03/06/2001	Rohit Kapur	SNSY-A2000-036	3674

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,841	KAPUR ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☑ The drawing(s) filed on 3/6/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because of the excess words.

Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 10, 17 and 25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "approximately more than" renders the claims indefinite, because the limitation does not properly define the lowest range of the pin capacity.

Claim Rej ctions - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-8, 11-15, 18-23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Motika et al. (US 5983380), issued: November 9, 1999.

Regarding independent Claims 1, 8, 15 and 22, Motika discloses an apparatus and method for a semiconductor integrated circuit device under test (DUT) 14 having a test scan arrangement, for communicating with a tester having a pin capacity through the shift register inputs (SRIs), which load patterns into the chip's shift register latches (SRLs) generated by the tester externally to the DUT 14, Figures 1 and 2, comprising:

Scan chains (128, 130, 132, 134, 136) and reconfiguration logic comprising a plurality of multiplexer (4:1 MUX 146) and a (2:1 MUX) coupled to the scan chains, where the logic selectively changes pin configuration required to test the DUT by reconfiguring the individual length and the number of scan chains based on the "mode select" signal from register 142 and "global weight set select" signal from register 138, where the logic provides the compatibility between the test patterns vectors generated

by the tester and the tester external to the DUT, where the first tester has a first pin capacity, when the "mode select" signal at logic level "0" allows the LSSD normal pin configuration and wherein the second tester has a second pin capacity, when the "mode select" signal at logic level "1" allows the WRPLBIST test mode pin configuration, FIGS. 2-4.

Regarding independent Claims 8, 15 and 22, in addition to the common limitations applied to claim 1 above, Motika further discloses a storage medium (array 152) which is loaded with the desired test vector set from the tester developed for a first tester having a first pin capacity.

Selecting modes using "mode select" at logic level "0" for selecting the LSSD normal pin configuration and "mode select" at logic level "1" for selecting the WRPLBIST test mode pin configuration, FIGS. 2-4.

A device under test DUT 14 for coupling with the first tester having a first pin capacity for receiving test vectors through the shift register inputs (SRI), FIG. 2.

Regarding Claim 4, 11, 18 and 26, Motika discloses reconfiguration logic comprising a plurality of multiplexer (4:1 MUX 146) and a (2:1 MUX) coupled to the scan chains between the selected chains (128, 130, 132, 134, 136) and the selected scan-in pins (SRIs) inputs to the DUT 14, FIG. 2.

Regarding Claim 5, 12, 19 and 27, Motika discloses reconfiguration logic comprising a functional input shift register (Linear Feedback Shift Register (LFSR) 12 for receiving SRI data or test vector 140 and for applying test vectors to integrated circuit device under test (DUT) 14 corresponding to the second tester having a second

pin capacity, and a functional output shift register such as multiple input signature register (MISR) 16 for providing output values corresponding to the second pin capacity.

Regarding Claim 6, 13, 20 and 28, Motika discloses reconfiguration logic, which also comprises a respective multiplexer (4:1 MUX 146), for each memory cell of the functional input shift register (12) for selecting between a respective memory cell and a respective functional input pin (SRI) based on the mode signal "global weight set select" signal from register 138, FIGS. 2-4.

Regarding Claim 7, 14, 21 and 29, Motika discloses a protocol unit (register 138) coupled to the mode signal "global weight set select" and further comprising a first test sequence "0" binary [00] used for the first tester having a first pin capacity, which allows the normal LSSD normal pin configuration and furthermore comprising a second test sequence "1" binary [01] used for the second tester having s second pin capacity, which allows the WRPLBIST test mode pin configuration, FIGS. 2-4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 9, 10, 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. (US 5983380) in view of Omura et al. (US 6311300).

Regarding Claims 2, 3, 9, 10, 16, 17, 24 and 25, Motika does not explicitly disclose that a second pin capacity is less than a first pin capacity and wherein the second pin capacity is approximately more than 64 pins and the first pin capacity is proximately more than 1000 pins. Omura et al. (US 6311300) discloses a semiconductor testing apparatus (50) for testing semiconductor device IC 70 having multiple pins including pin electronics 61 which interfaces with the DUT though contact terminal 71. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to test the multiple pin semiconductor device under test, as taught by Omura, in the automatic test equipment of Motika, since Motica provides a pin electronics unit which is flexible for interfacing between an ATE tester and a DUT having different pin capacity, thus avoiding the use of multiple tasters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: _____.

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 2/25/04
Non-Final Rejection

Guy J. Lamare
for

Albert DeCady
Primary Examiner